REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated January 23, 2009 has been received and its contents carefully reviewed.

Claims 1, 3, 8, 9, 11, 12, 14-27, 29, 30 and 32-34 are rejected. Applicant has amended claims 1, 3, 9 and 30, and deleted claims 32 and 34 to further define the invention. No new matter has been added.

The Office Actions rejects claims 1 and 8 under 35 U.S.C. 103(a) as being unpatentable over Cairn et al. ("Cairns1") (US Patent Application: 2002/0030653 A1) in view of Cairns et al. ("Cairns2")(US Patent No: 6,268,841 B1), Enami et al. (US Patent No: 5,892,493), and Morita (US Patent No: 6,989,810 B2), rejects claims 30 and 34 under 35 U.S.C. 103(a) as being unpatentable over Cairn et al. ("Cairns1") (US Patent Application: 2002/0030653 A1) in view of Cairns et al. ("Cairns2")(US Patent No: 6,268,841 B1), rejects claims 3 and 32 under 35 U.S.C. 103(a) as being unpatentable over Cairn et al. ("Cairns1") (US Patent Application: 2002/0030653 A1), in view of Cairns et al. ("Cairns2")(US Patent No: 6,268,841 B1) and Nitta et al. (US Patent No: 6,661,402 B1), and rejects claims 9, 14-29 under 35 U.S.C. 103(a) as being unpatentable over Cairn et al. ("Cairns1") (US Patent Application: 2002/0030653 A1), in view of Cairns et al. ("Cairns2")(US Patent No: 6,268,841 B1), Enami et al. (US Patent No: 5,892,493), Nitta et al. (US Patent No: 6,661,402 B1), and Morita (US Patent No: 6,989,810 B2). Reexamination and reconsideration of the pending claims are respectfully requested.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "a latch part sequentially latching a plurality of digital pixel data in response to the sampling signal from the shift register part; a first multiplexer part performing a time-division on the digital pixel data from the latch part, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; a digital-analog converter part including: a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal; and a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal; a demultiplexer part supplying the positive pixel signal from the positive digital-analog converter

and the negative pixel signal from the negative digital-analog converter to corresponding output channels during the first half of a horizontal period and during the second half of the horizontal period; and an output part including: a sampling part sampling the positive pixel signals and the negative pixel signals from the demultiplexer; a holding part holding the sampled pixel signals from the sampling part; and an output buffer part for buffering the held pixel signals from the holding part, and a second multiplexer part for simultaneously outputting the buffered pixel signals from the output buffer part in response to a source output enable signal during the next horizontal period following the horizontal period, wherein the first multiplexer and the demultiplexer part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period and a polarity control signal".

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "a latch part sequentially latching a plurality of digital pixel data in response to the sampling signal from the shift register part; a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; a level shifter part raising a voltage of the time-divided pixel data from the multiplexer part; a digital-analog converter part including: a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal; and a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal; a demultiplexer part providing the positive pixel signal from the positive digital-analog converter and the negative pixel signal received from the digital-analog converter to output channels of the demultiplexer corresponding to the data lines during the first half of the first horizontal period and during the second half of the first horizontal period; and an output part including: a sampling part sampling the positive pixel signals and the negative pixel signals from the demultiplexer; a holding part holding the sampled pixel signals provided through the sampling part; and a discharging part simultaneously outputting the pixel signals held in the holding part for the first horizontal period to corresponding data lines for an enable period of a source output enable signal of a second horizontal period and outputting a reference voltage to the corresponding data lines for a disable period of the source output enable signal of the second horizontal period".

Claim 30 is allowable over the cited references in that claim 30 recites a combination of elements including, for example, "performing a time-division on a plurality of digital pixel data for a first horizontal period, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal; supplying the positive pixel signal and the negative pixel signal to corresponding output channels; sampling and holding the positive pixel signals and the negative pixel signals; and simultaneously outputting the held pixel signals to corresponding data lines for an enable period of an input source output enable signal of a second horizontal period and outputting a reference voltage to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period".

None of the cited references, singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claims 1, 9 and 30 and claims 3, 8, 11, 12, 14-27 and 29, which respectively depend therefrom, are allowable over the cited references.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911.

Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

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